12. (Amended) The semiconductor die as recited in claim 11, wherein each planar perimeter side surface [has an entirely flat, smooth surface] is transverse to the first planar surface and the second planar surface.

13. The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. (Amended) The semiconductor die as recited in claim 11, wherein each planar perimeter surface [has] is a ground surface.

15. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface[; and

wherein at least one perimeter surface having a treated surface,] the entire at least one perimeter side surface having a [substantially smooth] ground or polished surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape.

16. (Amended) The semiconductor die as recited in claim 15, wherein each planar perimeter [entire] side surface [comprises a ground surface] is transverse to the first planar surface and the second planar surface.

17. (Amended) The semiconductor die as recited in claim 15, wherein [the entire] each planar

perimeter side surface comprises a polished surface.

18. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other[, where at least one of the two offset planar surfaces of at least one perimeter side surface are substantially flat and smooth] and ground or polished.

19. The semiconductor die as recited in claim 18, wherein the semiconductor die comprises a rectangular die.

20. The semiconductor die as recited in claim 18, wherein each perimeter side surface has offset planar surfaces.

21. (Amended) The semiconductor die as recited in claim 18, wherein [each offset planar surfaces is substantially smooth and flat] the at least two offset planar surfaces are transverse to the first planar surface and the second planar surface.

22. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface;

a layer of scribe material forming the planar perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

means for treating the at least one [or more of the] planar perimeter side [surfaces] surface of the semiconductor die to provide the at least one [or more of the] planar perimeter side [surfaces] surface with [one or more substantially treated, and smooth surfaces] a ground or polished surface.

23.(Amended) The semiconductor die as recited in claim 22, wherein each of the entire planar perimeter side [surface] surfaces extends between the first planar surface and the second planar surface and is a [substantially smooth] ground or polished surface.

24. (Amended) The semiconductor die as recited in claim 22, wherein the at least one planar perimeter side surface [has offset planar surfaces, where the planar surfaces are each substantially smooth and are substantially parallel to each other] is transverse to the first planar surface and the second planar surface.

25. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface;

each perimeter side surface having offset perimeter planar surfaces, where the perimeter planar surfaces are substantially parallel to each other, and each of the perimeter planar surfaces [are treated, substantially smooth] is a ground or polished surface [surfaces];

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the semiconductor die has an overall rectangular footprint.

35. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having two or more offset planar perimeter surfaces, [at least one perimeter side surface having a treated, substantially smooth surface] each of the two or more offset planar perimeter surfaces being ground or polished surfaces, where the planar perimeter surfaces are substantially transverse to the first planar surface and the second planar surface.

36. (Amended) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter [surface] surfaces is transverse to the first planar surface and the second planar surface [has an entirely flat, smooth surface].

37. The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.

38. (Amended) The semiconductor die as recited in claim 35, wherein the two or more offset planar perimeter surfaces [have ground surfaces] are parallel.

39. (Thrice Amended) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces [have] are polished surfaces.

40. (Amended) The semiconductor die as recited in claim 35, wherein each of the planar perimeter surfaces [are substantially parallel to one another] include two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces.

41. (Twice Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges transverse to and extending between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface; and

each offset planar surface [has a flat, smooth] having a ground or polished surface.

42. The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

43. The semiconductor die as recited in claim 41, wherein the offset planar surfaces are substantially parallel to one another.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 25, 2002, and the references cited therewith. Claims 11, 12, 14-18, 21-25, 35, 36 and 38-41 are amended such that claims 11-25 and 35-43 are now pending in this application.

§102 Rejection of the Claims

Claims 11-25 and 35-43 were rejected under 35 USC § 102(b) as being anticipated by Ormond et al. (U.S. Patent No. 5,128,282). "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." (emphasis added). *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).